

```

RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 23
description:
top level BOM
-----
revision 3.828
date: 1995/06/08 19:44:20;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        wbck_debug.sig

Added fillstate to trace.
-----
revision 3.827
date: 1995/06/08 17:47:54;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        uu_debug.srl

Fix signal name, again
-----
revision 3.826
date: 1995/06/08 17:27:00;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        uu_debug.srl

Fix signal names
-----
revision 3.825
date: 1995/06/08 13:46:38;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

m13 - > m16
-----
revision 3.824
date: 1995/06/07 23:17:20;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.
-----
revision 3.823
date: 1995/06/07 22:40:41;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
    A cylinder doing an I fill interrupted away so that forward progress became
    active.  This allowed another cyl to start a new I miss, which reloaded
    the saved GVA needed to write the original miss's ITag entry.  Delays in

```

the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
So change CC to release inprog(p1) not when it sees the last I fill hexlet get
stuffed into NB (which was arbitrarily modeled upon the same main pipe point
when the DCache/DTag get written directly on D fills), but instead when CP
confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

revision 3.822
date: 1995/06/07 22:30:35; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Added more signals to uu_debug.srl.

revision 3.821
date: 1995/06/07 18:56:49; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 3.820
date: 1995/06/07 17:57:45; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Modernized and added ifetch snake path stuff.

revision 3.819
date: 1995/06/07 16:44:21; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
lva_debug.sig

For debugging lva calculations.

revision 3.818
date: 1995/06/07 05:29:55; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
template

More variations

revision 3.817
date: 1995/06/06 20:18:01; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

Delete extra space causing missing seperator

revision 3.816
date: 1995/06/06 20:05:36; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

Build variations with differnet octlet 10 dram values

revision 3.815
date: 1995/06/06 19:47:42; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/include

Added set_ratio_m1 and set_ratio_m1_6 macros

revision 3.814

date: 1995/06/06 18:02:50; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/hc

hc0_control.pim

Move usnapi2/u0 to avoid a toplevel collision

revision 3.813

date: 1995/06/06 16:00:37; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 3.812

date: 1995/06/06 02:27:15; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

cc/cclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:

On latedirty cases that CC calls "ahd" (store issues at later time than instr causing D miss), the start vldStr were correctly pipelined to R16 and R18 for cclatedirty.Veqn to examine but not the match result which was staged to R14 only then used in R16 and R18. This caused matches from the cyl number 2 higher for the -2 case and 4 higher for the -4 case to be used instead of our own cylinder. Test hermnasty_1 accidentally noticed. Fix in cc.V 1.83 was probably never right but just perturbed cachesynchnasty2_var_a_1 enough to make it pass.

cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.

Also note that ccrcv.Veqn 51.7 logmsg should have noted that it was making the I inprog release 10 ticks later as it already was in the D case to prevent CC from absorbing a new D miss too quickly after an I miss finished. The new D miss would retrigger the still piping later vldFillR21 causing the fillcount to get out of synch with the rest of CC, allowing CC to think it was done 1 hexlet early on later fills and clobber registers holding the write data for the 4th hexlet fill. Test exintbash_var_a_1 accidentally noticed.

euterpe.V: Change net names from

HZtCdNdxHzrdS9S12L5L6 HZtCdNdxHzrdS5S8L5L6 HZtCdNdxHzrdS1S4L9L10 to

HZtCdNdxHzrdS11S14L5L6 HZtCdNdxHzrdS7S10L5L6 HZtCdNdxHzrdS5S8L9L10

to reflect actual staging. At least the wbck.srl will have to be updated to match.

revision 3.811

date: 1995/06/05 22:35:17; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 3.810

date: 1995/06/05 21:40:56; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Makefile

euterpe.V

Makefile: Revert wrapchsim & ch_euterpe_wrap.v back to non-real regfile & gtlb.

euterpe.V: Change net name CDdInS17S20 to CDdInS16S19 to reflect actual

staging. At least the dbuf.srl will have to be updated to match.

revision 3.809

date: 1995/06/05 19:12:46; author: doi; state: Exp; lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

enable dram and add support for gcopyswap11i

revision 3.808

date: 1995/06/05 17:06:01; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 3.807

date: 1995/06/04 05:22:18; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/include

Release new dram macros.

revision 3.806

date: 1995/06/03 14:52:39; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row innmed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nba16x64/spice.1.3,v

Working file: ged/rf/nba16x64/spice.1.3

head: 1.2

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 2; selected revisions: 1

description:

revision 1.2

date: 1995/06/04 01:26:19; author: ong; state: Exp; lines: +1339 -1339

Replaced output with full swing FF

=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nba16x64/spice.1.4,v

Working file: ged/rf/nba16x64/spice.1.4

head: 1.3

branch:

locks: strict

access list:

keyword substitution: kv

```

total revisions: 3;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/06/04 01:26:30;  author: ong;  state: Exp;  lines: +448 -448
Replaced output with full swing FF
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nba16x64/spice_cn.1.3,v
Working file: ged/rf/nba16x64/spice_cn.1.3
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/06/04 01:26:33;  author: ong;  state: Exp;  lines: +501 -501
Replaced output with full swing FF
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nba16x64/spice_cn.1.4,v
Working file: ged/rf/nba16x64/spice_cn.1.4
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/06/04 01:26:36;  author: ong;  state: Exp;  lines: +168 -168
Replaced output with full swing FF
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nbd32x64/spice.1.3,v
Working file: ged/rf/nbd32x64/spice.1.3
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/06/04 01:27:17;  author: ong;  state: Exp;  lines: +1340 -1336
Replaced half swing output FF with full swing
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nbd32x64/spice.1.4,v
Working file: ged/rf/nbd32x64/spice.1.4
head: 1.3
branch:

```

```

locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/06/04 01:27:27;  author: ong;  state: Exp;  lines: +412 -412
Replaced half swing output FF with full swing
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nbd32x64/spice_cn.1.3,v
Working file: ged/rf/nbd32x64/spice_cn.1.3
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/06/04 01:27:31;  author: ong;  state: Exp;  lines: +501 -500
Replaced half swing output FF with full swing
=====

RCS file: /s6/cvsroot/euterpe/ged/rf/nbd32x64/spice_cn.1.4,v
Working file: ged/rf/nbd32x64/spice_cn.1.4
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/06/04 01:27:34;  author: ong;  state: Exp;  lines: +163 -163
Replaced half swing output FF with full swing
=====

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;     selected revisions: 18
description:
-----
revision 4.173
date: 1995/06/08 19:43:54;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                wbck_debug.sig

Added fillstate to trace.

```

revision 4.172
date: 1995/06/08 17:47:31; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Fix signal name, again

revision 4.171
date: 1995/06/08 17:26:36; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Fix signal names

revision 4.170
date: 1995/06/08 13:46:19; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
template

m13 - > m16

revision 4.169
date: 1995/06/07 23:17:02; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.168
date: 1995/06/07 22:30:16; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Added more signals to uu_debug.srl.

revision 4.167
date: 1995/06/07 18:56:27; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.166
date: 1995/06/07 17:57:16; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Modernized and added ifetch snake path stuff.

revision 4.165
date: 1995/06/07 16:44:00; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
lva_debug.sig

For debugging lva calculations.

revision 4.164
date: 1995/06/07 05:29:40; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel
template

More variations

revision 4.163
date: 1995/06/06 20:17:45; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

Delete extra space causing missing seperator

revision 4.162
date: 1995/06/06 20:05:19; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

Build variations with differnet octlet 10 dram values

revision 4.161
date: 1995/06/06 19:47:26; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/include

Added set_ratio_m1 and set_ratio_m1_6 macros

revision 4.160
date: 1995/06/06 16:00:14; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.159
date: 1995/06/05 22:34:46; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.158
date: 1995/06/05 19:12:18; author: doi; state: Exp; lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

enable dram and add support for gcopyswap11i

revision 4.157
date: 1995/06/05 17:05:42; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.156
date: 1995/06/04 05:21:57; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/include

Release new dram macros.

=====
RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v
Working file: verify/include/BOM
head: 36.0


```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 4
description:
releasebom adding BOM
-----
revision 33.0
date: 1995/06/06 19:47:16;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include

Added set_ratio_m1 and set_ratio_m1_6 macros
-----
revision 32.1
date: 1995/06/06 19:47:10;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 32.0
date: 1995/06/04 05:21:46;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include

Release new dram macros.
-----
revision 31.1
date: 1995/06/04 05:21:38;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/include/cerberus.h,v
Working file: verify/include/cerberus.h
head: 10.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
-----
revision 10.19
date: 1995/06/06 19:46:50;  author: lisar;  state: Exp;  lines: +38 -1
Added set_ratio_m1 and set_ratio_m1_6 macros
-----
revision 10.18
date: 1995/06/04 05:21:02;  author: lisar;  state: Exp;  lines: +51 -1
Added macros clobber_refresh_mult, increase_refresh_mult and set_m1_3.
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/BOM,v
Working file: verify/nasty/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 36;    selected revisions: 4
description:

```

```

releasebom adding BOM
-----
revision 16.0
date: 1995/06/06 20:17:34; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/nasty

Delete extra space causing missing seperator
-----
revision 15.1
date: 1995/06/06 20:17:28; author: lisar; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 15.0
date: 1995/06/06 20:05:09; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/nasty

Build variations with differnet octlet 10 dram values
-----
revision 14.1
date: 1995/06/06 20:05:03; author: lisar; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/Makefile,v
Working file: verify/nasty/Makefile
head: 1.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14; selected revisions: 3
description:
-----
revision 1.11
date: 1995/06/06 20:16:26; author: lisar; state: Exp; lines: +2 -2
Delete extrac space couising missing seperator
-----
revision 1.10
date: 1995/06/06 19:46:01; author: lisar; state: Exp; lines: +69 -54
Added variations that turn on refresh, increash the refresh rate and
decrease m1 ratio.
-----
revision 1.9
date: 1995/06/04 05:19:34; author: lisar; state: Exp; lines: +152 -3
Added varations with refresh, fast refresh and fast dram interface.
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5.S,v
Working file: verify/nasty/cachenasty5.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 2
description:
-----

```

```

revision 1.5
date: 1995/06/06 19:46:03; author: lisar; state: Exp; lines: +3 -3
Added variations that turn on refresh, increash the refresh rate and
decrease m1 ratio.
-----
revision 1.4
date: 1995/06/04 05:19:36; author: lisar; state: Exp; lines: +10 -1
Added varations with refresh, fast refresh and fast dram interface.
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2.S,v
Working file: verify/nasty/cachesynchnasty2.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 2
description:
-----
revision 1.6
date: 1995/06/06 19:46:05; author: lisar; state: Exp; lines: +3 -3
Added variations that turn on refresh, increash the refresh rate and
decrease m1 ratio.
-----
revision 1.5
date: 1995/06/04 05:19:37; author: lisar; state: Exp; lines: +10 -1
Added varations with refresh, fast refresh and fast dram interface.
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/exintbash.S,v
Working file: verify/nasty/exintbash.S
head: 3.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 3.4
date: 1995/06/06 19:46:06; author: lisar; state: Exp; lines: +10 -1
Added variations that turn on refresh, increash the refresh rate and
decrease m1 ratio.
=====

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;    selected revisions: 1
description:
-----
revision 1.166

```

date: 1995/06/05 06:21:38; author: lisar; state: Exp; lines: +55 -4
Turn on refresh and increase timing.

=====
RCS file: /s6/cvsroot/euterpe/verify/obj/system/nasty/Makefile,v
Working file: verify/obj/system/nasty/Makefile
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16; selected revisions: 3
description:

revision 1.11

date: 1995/06/06 20:16:26; author: lisar; state: Exp; lines: +2 -2
Delete extrac space cousing missing seperator

revision 1.10

date: 1995/06/06 19:46:01; author: lisar; state: Exp; lines: +69 -54
Added variations that turn on refresh, increash the refresh rate and
decrease m1 ratio.

revision 1.9

date: 1995/06/04 05:19:34; author: lisar; state: Exp; lines: +152 -3
Added varations with refresh, fast refresh and fast dram interface.

=====
RCS file: /s6/cvsroot/euterpe/verify/perf/Makefile,v
Working file: verify/perf/Makefile
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10; selected revisions: 1
description:

revision 1.4

date: 1995/06/07 22:27:03; author: lisar; state: Exp; lines: +12 -2
Added new tests

=====
RCS file: /s6/cvsroot/euterpe/verify/perf/bgate_perf.S,v
Working file: verify/perf/bgate_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1

date: 1995/06/06 22:35:45; author: claseman; state: Exp;
initial revision

RCS file: /s6/cvsroot/euterpe/verify/perf/bgatEI_perf.S,v
Working file: verify/perf/bgatEI_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1
date: 1995/06/06 22:35:48; author: claseman; state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/bi_perf.S,v
Working file: verify/perf/bi_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1
date: 1995/06/06 22:35:49; author: claseman; state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress16_perf.S,v
Working file: verify/perf/gcompress16_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:

revision 3.1
date: 1995/06/08 22:16:37; author: claseman; state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress64_perf.S,v
Working file: verify/perf/gcompress64_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:

revision 3.1

date: 1995/06/08 22:16:40; author: claseman; state: Exp;
initial revision

=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gmdepil_perf.S,v
Working file: verify/perf/gmdepil_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1
date: 1995/06/08 22:16:42; author: claseman; state: Exp;
initial revision

=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gmdepi64_perf.S,v
Working file: verify/perf/gmdepi64_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1
date: 1995/06/08 22:16:45; author: claseman; state: Exp;
initial revision

=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gselect8_perf.S,v
Working file: verify/perf/gselect8_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 3.1
date: 1995/06/08 22:16:47; author: claseman; state: Exp;
initial revision

=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gsete64_perf.S,v
Working file: verify/perf/gsete64_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1

```

description:
-----
revision 3.1
date: 1995/06/06 22:35:51;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/gtranspose8mux_perf.S,v
Working file: verify/perf/gtranspose8mux_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/08 22:16:49;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/lu32li_perf.S,v
Working file: verify/perf/lu32li_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/08 22:16:51;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/lu8i_perf.S,v
Working file: verify/perf/lu8i_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/08 22:16:53;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/mbnez_perf.S,v
Working file: verify/perf/mbnez_perf.S
head: 3.2
branch:
locks: strict

```

```

access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/08 22:16:55;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/saas64la_perf.S,v
Working file: verify/perf/saas64la_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/06 22:35:53;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/smas64la_perf.S,v
Working file: verify/perf/smas64la_perf.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/06 22:35:55;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/random/Makefile,v
Working file: verify/random/Makefile
head: 1.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;     selected revisions: 3
description:
-----
revision 1.18
date: 1995/06/08 16:32:10;  author: dit00;   state: Exp;   lines: +5 -5
Removed incorrect \'s in stgen and stbash
-----
revision 1.17
date: 1995/06/07 23:10:14;  author: lisar;   state: Exp;   lines: +30 -9
Added stbash rules

```



```
-----
revision 1.16
date: 1995/06/05 18:16:37;  author: dit00;  state: Exp;  lines: +3 -11
*** empty log message ***
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2279.S,v
Working file: verify/random/regdepend_r2279.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
```

```
revision 3.1
date: 1995/06/05 18:12:15;  author: dit00;  state: Exp;
Test Ran_OK.]
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2476.S,v
Working file: verify/random/regdepend_r2476.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
```

```
revision 3.1
date: 1995/06/05 18:18:01;  author: dit00;  state: Exp;
*** empty log message ***
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2493.S,v
Working file: verify/random/regdepend_r2493.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
```

```
revision 3.1
date: 1995/06/06 14:46:37;  author: dit00;  state: Exp;
Test Ran_OK
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2688.S,v
Working file: verify/random/regdepend_r2688.S
head: 3.2
branch:
locks: strict
access list:
```

```

keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/05 18:18:15;  author: dit00;  state: Exp;
*** empty log message ***
=====

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2695.S,v
Working file: verify/random/regdepend_r2695.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/06 14:47:01;  author: dit00;  state: Exp;
Test Ran_OK
=====

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2895.S,v
Working file: verify/random/regdepend_r2895.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/05 18:18:19;  author: dit00;  state: Exp;
*** empty log message ***
=====

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3094.S,v
Working file: verify/random/regdepend_r3094.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/05 18:18:23;  author: dit00;  state: Exp;
*** empty log message ***
=====

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3362.S,v
Working file: verify/random/regdepend_r3362.S
head: 3.2

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/06/07 14:22:23;  author: dit00;  state: Exp;
Test ran ok
=====

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;      selected revisions: 4
description:
-----
revision 2.8
date: 1995/06/06 14:47:19;  author: dit00;  state: Exp;  lines: +1 -0
Update status
-----
revision 2.7
date: 1995/06/06 14:20:05;  author: dit00;  state: Exp;  lines: +5 -0
status update
-----
revision 2.6
date: 1995/06/05 18:18:27;  author: dit00;  state: Exp;  lines: +5 -0
Test Ran_OK.
-----
revision 2.5
date: 1995/06/05 17:56:03;  author: dit00;  state: Exp;  lines: +7 -0
Update status file
=====

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;      selected revisions: 2
description:
-----
revision 2.7
date: 1995/06/06 14:47:39;  author: dit00;  state: Exp;  lines: +4 -5
Update to reflect latest test status
-----
revision 2.6
date: 1995/06/05 18:18:49;  author: dit00;  state: Exp;  lines: +85 -0
Test Ran_OK.
=====

```

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v

Working file: verify/tools/BOM

head: 13.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 90; selected revisions: 1

description:

releasebom adding BOM

revision 7.3

date: 1995/06/05 19:12:02; author: doi; state: Exp; lines: +2 -2

Release Target: euterpe/verify/tools/regdepend

enable dram and add support for gcopyswap11i

=====

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/BOM,v

Working file: verify/tools/regdepend/BOM

head: 26.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 50; selected revisions: 2

description:

releasebom adding BOM

revision 24.0

date: 1995/06/05 19:11:48; author: doi; state: Exp; lines: +1 -1

Release Target: euterpe/verify/tools/regdepend

enable dram and add support for gcopyswap11i

revision 23.1

date: 1995/06/05 19:11:38; author: doi; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/regdepend.c,v

Working file: verify/tools/regdepend/regdepend.c

head: 1.29

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 29; selected revisions: 1

description:

revision 1.27

date: 1995/06/05 19:11:07; author: doi; state: Exp; lines: +16 -4

enable dram and add support for gcopyswap11i

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v

```

Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 13
description:
releasebom adding BOM
-----
revision 39.31
date: 1995/06/08 19:43:38;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                wbck_debug.sig

Added fillstate to trace.
-----
revision 39.30
date: 1995/06/08 17:47:19;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                uu_debug.srl

Fix signal name, again
-----
revision 39.29
date: 1995/06/08 17:26:24;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                uu_debug.srl

Fix signal names
-----
revision 39.28
date: 1995/06/08 13:46:09;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                template

m13 - > m16
-----
revision 39.27
date: 1995/06/07 23:16:51;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.
-----
revision 39.26
date: 1995/06/07 22:29:59;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                uu_debug.srl

Added more signals to uu_debug.srl.
-----
revision 39.25
date: 1995/06/07 18:56:15;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.
-----

```

revision 39.24
date: 1995/06/07 17:57:01; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
uu_debug.srl

Modernized and added ifetch snake path stuff.

revision 39.23
date: 1995/06/07 16:43:49; author: jeffm; state: Exp; lines: +5 -1
Release Target: euterpe/verify/toplevel
lva_debug.sig

For debugging lva calculations.

revision 39.22
date: 1995/06/07 05:29:31; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
template

More variations

revision 39.21
date: 1995/06/06 16:00:00; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 39.20
date: 1995/06/05 22:34:27; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 39.19
date: 1995/06/05 17:05:31; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

=====
RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185; selected revisions: 1
description:

revision 1.166
date: 1995/06/05 06:21:38; author: lisar; state: Exp; lines: +55 -4
Turn on refresh and increase timing.

=====
RCS file: /s6/cvsroot/euterpe/verify/toplevel/dbuf_debug.sig,v
Working file: verify/toplevel/dbuf_debug.sig

```

head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 39.1
date: 1995/06/04 22:19:12;  author: lisar;  state: Exp;
Used in exintbash_var_a_1 debug
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ibufhz_debug.srl,v
Working file: verify/toplevel/ibufhz_debug.srl
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 39.1
date: 1995/06/06 22:19:59;  author: lisar;  state: Exp;
Ibuffer hazard
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/latedirty.S,v
Working file: verify/toplevel/latedirty.S
head: 37.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 2
description:
-----
revision 37.4
date: 1995/06/07 18:36:59;  author: jeffm;  state: Exp;  lines: +49 -5
Due to a bug in the looping algo, was only doing 1/4th of the cases.

Per mws, make the cylinders that are not involved in the latedirty case
do ecopyi's that will generate an index in the pipe that the involved
cylinders do not use.
-----
revision 37.3
date: 1995/06/06 20:38:10;  author: jeffm;  state: Exp;  lines: +21 -3
Fixed the following:

Unique data patterns, so that missing wbocks can be detected.

Set page size to 8K to avoid page crossers in timing sensitive areas.

Make absolutely sure that the clean line is in the cache at the start of
each case.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/toplevel/lva_debug.sig,v
Working file: verify/toplevel/lva_debug.sig
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 39.2
date: 1995/06/07 18:55:30;  author: lisar;  state: Exp;  lines: +0 -1
Deleted /uut/euterpe/RGopbRegBenRQ as not found in design
-----
revision 39.1
date: 1995/06/07 16:43:06;  author: jeffm;  state: Exp;
For debugging lva calculations.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/store_unique.S,v
Working file: verify/toplevel/store_unique.S
head: 7.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;      selected revisions: 1
description:
-----
revision 7.13
date: 1995/06/05 06:21:40;  author: lisar;  state: Exp;  lines: +13 -1
Turn on refresh and increase timing.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;      selected revisions: 3
description:
-----
revision 1.107
date: 1995/06/08 13:44:32;  author: lisar;  state: Exp;  lines: +28 -22
m13 - > m16
-----
revision 1.106
date: 1995/06/07 05:29:05;  author: lisar;  state: Exp;  lines: +20 -19
More variations
-----
revision 1.105
date: 1995/06/05 06:21:45;  author: lisar;  state: Exp;  lines: +123 -55
Turn on refresh and increase timing.
=====

```



```

RCS file: /s6/cvsroot/euterpe/verify/toplevel/uu_debug.srl,v
Working file: verify/toplevel/uu_debug.srl
head: 5.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;      selected revisions: 4
description:
-----
revision 5.5
date: 1995/06/08 17:46:52;  author: jeffm;  state: Exp;  lines: +2 -2
Fix signal name.
-----
revision 5.4
date: 1995/06/08 17:25:54;  author: jeffm;  state: Exp;  lines: +12 -12
Fix instance name for holduu.
-----
revision 5.3
date: 1995/06/07 22:29:11;  author: jeffm;  state: Exp;  lines: +15 -0
Added ibuf dout pins and we.
-----
revision 5.2
date: 1995/06/07 17:55:54;  author: jeffm;  state: Exp;  lines: +70 -163
Modernized and added ifetch snake path stuff.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/wbck_debug.sig,v
Working file: verify/toplevel/wbck_debug.sig
head: 33.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;      selected revisions: 1
description:
-----
revision 33.9
date: 1995/06/08 19:43:03;  author: jeffm;  state: Exp;  lines: +2 -1
Added fillstate to trace.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/BOM,v
Working file: verify/toplevel/hermes/BOM
head: 12.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;      selected revisions: 10
description:
releasebom adding BOM
-----
revision 9.0
date: 1995/06/07 23:16:37;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

```

Fix hermetest.

revision 8.1

date: 1995/06/07 23:16:30; author: jeffm; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 8.0

date: 1995/06/07 18:56:00; author: jeffm; state: Exp; lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 7.1

date: 1995/06/07 18:55:50; author: jeffm; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 7.0

date: 1995/06/06 15:59:44; author: jeffm; state: Exp; lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 6.1

date: 1995/06/06 15:59:36; author: jeffm; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 6.0

date: 1995/06/05 22:34:06; author: jeffm; state: Exp; lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 5.1

date: 1995/06/05 22:33:49; author: jeffm; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 5.0

date: 1995/06/05 17:05:21; author: jeffm; state: Exp; lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

Fix hermetest.

revision 4.1

date: 1995/06/05 17:05:14; author: jeffm; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermetest.S,v

Working file: verify/toplevel/hermes/hermetest.S

head: 1.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 5

description:

revision 1.6
date: 1995/06/07 23:15:43; author: jeffm; state: Exp; lines: +8 -5
Not initializing enough itag entries.

revision 1.5
date: 1995/06/07 18:54:49; author: jeffm; state: Exp; lines: +11 -11
Raise test case priority to avoid ltlb misses.

revision 1.4
date: 1995/06/06 15:58:27; author: jeffm; state: Exp; lines: +2 -2
Fixed error in gtlb initialization.

revision 1.3
date: 1995/06/05 22:31:46; author: jeffm; state: Exp; lines: +3 -1
Dtag init loop was never-ending - got ex11.

revision 1.2
date: 1995/06/05 17:04:02; author: jeffm; state: Exp; lines: +2 -2
Fixed expected offchip addition result to be 0x14dc.
=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 5
description:
top level verilog BOM

revision 3.619
date: 1995/06/07 22:40:22; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
A cylinder doing an I fill interrupted away so that forward progress became
active. This allowed another cyl to start a new I miss, which reloaded
the saved GVA needed to write the original miss's ITag entry. Delays in
the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
So change CC to release inprog(p1) not when it sees the last I fill hexlet get
stuffed into NB (which was arbitrarily modeled upon the same main pipe point
when the DCache/DTag get written directly on D fills), but instead when CP
confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

revision 3.618
date: 1995/06/06 18:02:26; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
hc0_control.pim

Move usnapc2/u0 to avoid a toplevel collision

revision 3.617

date: 1995/06/06 02:26:58; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

cc/cclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:

On latedirty cases that CC calls "ahd" (store issues at later time than instr causing D miss), the start vldStr were correctly pipelined to R16 and R18 for cclatedirty.Veqn to examine but not the match result which was staged to R14 only then used in R16 and R18. This caused matches from the cyl number 2 higher for the -2 case and 4 higher for the -4 case to be used instead of our own cylinder. Test hermnasty_1 accidentally noticed. Fix in cc.V 1.83 was probably never right but just perturbed cachesynchnasty2_var_a_1 enough to make it pass.

cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.

Also note that ccrcv.Veqn 51.7 logmsg should have noted that it was making the I inprog release 10 ticks later as it already was in the D case to prevent CC from absorbing a new D miss too quickly after an I miss finished. The new D miss would retrigger the still piping later vldFillR21 causing the fillcount to get out of synch with the rest of CC, allowing CC to think it was done 1 hexlet early on later fills and clobber registers holding the write data for the 4th hexlet fill. Test exintbash_var_a_1 accidentally noticed.

euterpe.V: Change net names from

HZtCdNdxHzrdS9S12L5L6 HZtCdNdxHzrdS5S8L5L6 HZtCdNdxHzrdS1S4L9L10 to
HZtCdNdxHzrdS11S14L5L6 HZtCdNdxHzrdS7S10L5L6 HZtCdNdxHzrdS5S8L9L10
to reflect actual staging. At least the wbck.srl will have to be updated
to match.

revision 3.616

date: 1995/06/05 21:40:33; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Makefile
euterpe.V

Makefile: Revert wrapchsim & ch_euterpe_wrap.v back to non-real regfile & gtlb.

euterpe.V: Change net name CDdInS17S20 to CDdInS16S19 to reflect actual
staging. At least the dbuf.srl will have to be updated to match.

revision 3.615

date: 1995/06/03 14:52:24; author: woody; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Changes to euterpe.V and gt.V to accomodate for the 2 added vref signals to the gtlb. gt placement updated. The 2 vref generators are placed in the row immed below the gtlb with one on each side of the clockspar in the middle of the gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v

Working file: verilog/bsrc/BOM

head: 346.6

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 8
description:
-----
revision 318.0
date: 1995/06/07 22:40:01;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active.  This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry.  Delays in
  the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
  So change CC to release inprog(p1) not when it sees the last I fill hexlet get
  stuffed into NB (which was arbitrarily modeled upon the same main pipe point
  when the DCache/DTag get written directly on D fills), but instead when CP
  confirms that the ITag write is committed enough to let CC restart.
  Test cachennasty5_var_dr_1 accidentally noticed.
-----
revision 317.2
date: 1995/06/07 22:39:47;  author: mws;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
-----
revision 317.1
date: 1995/06/06 18:02:01;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
  hc0_control.pim

Move usnapc2/u0 to avoid a toplevel collision
-----
revision 317.0
date: 1995/06/06 02:26:38;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/ccclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:
  On latedirty cases that CC calls "ahd" (store issues at later time than
  instr causing D miss), the start vldStr were correctly pipelined to R16
  and R18 for ccclatedirty.Veqn to examine but not the match result which
  was staged to R14 only then used in R16 and R18.  This caused matches
  from the cyl number 2 higher for the -2 case and 4 higher for the -4 case
  to be used instead of our own cylinder.  Test hermnasty_1 accidentally
  noticed.  Fix in cc.V 1.83 was probably never right but just perturbed
  cachesynchnasty2_var_a_1 enough to make it pass.
cc/ccrcv.Veqn:  Add some comments explaining why CC releases when it does.
  Also note that ccrcv.Veqn 51.7 logmsg should have noted that
  it was making the I inprog release 10 ticks later as it already was in
  the D case to prevent CC from absorbing a new D miss too quickly after
  an I miss finished.  The new D miss would retrigger the still piping
  later vldFillR21 causing the fillcount to get out of synch with the rest
  of CC, allowing CC to think it was done 1 hexlet early on later fills
  and clobber registers holding the write data for the 4th hexlet fill.

```

```

Test exintbash_var_a_1 accidentally noticed.
euterpe.V: Change net names from
  HZtCdNdxHzrdS9S12L5L6 HZtCdNdxHzrdS5S8L5L6 HZtCdNdxHzrdS1S4L9L10 to
  HZtCdNdxHzrdS11S14L5L6 HZtCdNdxHzrdS7S10L5L6 HZtCdNdxHzrdS5S8L9L10
  to reflect actual staging. At least the wbcx.srl will have to be updated
  to match.
-----
revision 316.2
date: 1995/06/06 02:26:25; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 316.1
date: 1995/06/05 21:40:08; author: mws; state: Exp; lines: +3 -3
Release Target: euterpe/verilog/bsrc
  Makefile
  euterpe.V

Makefile: Revert wrapchsim & ch_euterpe_wrap.v back to non-real regfile & gtlb.
euterpe.V: Change net name CDdInS17S20 to CDdInS16S19 to reflect actual
  staging. At least the dbuf.srl will have to be updated to match.
-----
revision 316.0
date: 1995/06/03 14:52:06; author: woody; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.
-----
revision 315.1
date: 1995/06/03 14:51:53; author: woody; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255; selected revisions: 2
description:
-----
revision 1.247
date: 1995/06/05 21:39:12; author: mws; state: Exp; lines: +11 -9
Makefile: Revert wrapchsim & ch_euterpe_wrap.v back to non-real regfile & gtlb.
euterpe.V: Change net name CDdInS17S20 to CDdInS16S19 to reflect actual
  staging. At least the dbuf.srl will have to be updated to match.
-----
revision 1.246

```

date: 1995/06/03 14:45:00; author: woody; state: Exp; lines: +3 -3
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof

head: 307.11

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 11; selected revisions: 1

description:

revision 307.4

date: 1995/06/06 14:21:58; author: tbr; state: Exp; lines: +87762 -87755
from BOM 317 top level placement

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v

Working file: verilog/bsrc/chip_euterpe-base.xrf

head: 307.11

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 11; selected revisions: 1

description:

revision 307.4

date: 1995/06/06 14:25:28; author: tbr; state: Exp; lines: +42858 -42814
from BOM 317 top level placement

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v

Working file: verilog/bsrc/euterpe.V

head: 6.431

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 431; selected revisions: 4

description:

revision 6.425

date: 1995/06/07 22:28:21; author: mws; state: Exp; lines: +6 -6

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UVvldSN128WrtR10 UVvldSN128WrtDR10 name/function change) \

```
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active. This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry. Delays in
  the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
  So change CC to release inprog(pl) not when it sees the last I fill hexlet get
  stuffed into NB (which was arbitrarily modeled upon the same main pipe point
  when the DCache/DTag get written directly on D fills), but instead when CP
  confirms that the ITag write is committed enough to let CC restart.
  Test cachenasly5_var_dr_1 accidentally noticed.
```

```
-----
revision 6.424
date: 1995/06/06 02:17:45; author: mws; state: Exp; lines: +12 -12
euterpe.V: Change net names from
  HZtCdNdxHzrdS9S12L5L6 HZtCdNdxHzrdS5S8L5L6 HZtCdNdxHzrdS1S4L9L10 to
  HZtCdNdxHzrdS11S14L5L6 HZtCdNdxHzrdS7S10L5L6 HZtCdNdxHzrdS5S8L9L10
  to reflect actual staging. At least the wbck.srl will have to be updated
  to match.
```

```
-----
revision 6.423
date: 1995/06/05 21:39:19; author: mws; state: Exp; lines: +19 -19
Makefile: Revert wrapchsim & ch_euterpe_wrap.v back to non-real regfile & gtlb.
euterpe.V: Change net name CDdInS17S20 to CDdInS16S19 to reflect actual
  staging. At least the dbuf.srl will have to be updated to match.
```

```
-----
revision 6.422
date: 1995/06/03 14:45:05; author: woody; state: Exp; lines: +5 -1
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.
```

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182; selected revisions: 4
description:
releasebom adding BOM
```

```
-----
revision 90.0
date: 1995/06/07 22:30:47; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
```


A cylinder doing an I fill interrupted away so that forward progress became active. This allowed another cyl to start a new I miss, which reloaded the saved GVA needed to write the original miss's ITag entry. Delays in the fill writes navigating through NB+CP allowed the fill adrs to change 1st. So change CC to release inprog(p1) not when it sees the last I fill hexlet get stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart.
 Test cachennasty5_var_dr_1 accidentally noticed.

```
-----
revision 89.1
date: 1995/06/07 22:30:40; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
```

```
revision 89.0
date: 1995/06/06 02:19:25; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
cc/cclatedirty.Vegn cc/cc.V cc/cc_control_blob.pim:
  On latedirty cases that CC calls "ahd" (store issues at later time than
  instr causing D miss), the start vldStr were correctly pipelined to R16
  and R18 for cclatedirty.Vegn to examine but not the match result which
  was staged to R14 only then used in R16 and R18. This caused matches
  from the cyl number 2 higher for the -2 case and 4 higher for the -4 case
  to be used instead of our own cylinder. Test hermnasty_1 accidentally
  noticed. Fix in cc.V 1.83 was probably never right but just perturbed
  cachesynchnasty2_var_a_1 enough to make it pass.
cc/ccrcv.Vegn: Add some comments explaining why CC releases when it does.
  Also note that ccrcv.Vegn 51.7 logmsg should have noted that
  it was making the I inprog release 10 ticks later as it already was in
  the D case to prevent CC from absorbing a new D miss too quickly after
  an I miss finished. The new D miss would retrigger the still piping
  later vldFillR21 causing the fillcount to get out of synch with the rest
  of CC, allowing CC to think it was done 1 hexlet early on later fills
  and clobber registers holding the write data for the 4th hexlet fill.
  Test exintbash_var_a_1 accidentally noticed.
euterpe.V: Change net names from
  HZtCdNdxHzrdsS9S12L5L6 HZtCdNdxHzrdsS5S8L5L6 HZtCdNdxHzrdsS1S4L9L10 to
  HZtCdNdxHzrdsS11S14L5L6 HZtCdNdxHzrdsS7S10L5L6 HZtCdNdxHzrdsS5S8L9L10
  to reflect actual staging. At least the wbck.srl will have to be updated
  to match.
```

```
-----
revision 88.1
date: 1995/06/06 02:19:17; author: mws; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
Working file: verilog/bsrc/cc/cc.V
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87; selected revisions: 2
description:
-----
```

```

revision 1.86
date: 1995/06/07 22:28:56; author: mws; state: Exp; lines: +24 -21
cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active. This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry. Delays in
  the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
  So change CC to release inprog(p1) not when it sees the last I fill hexlet get
  stuffed into NB (which was arbitrarily modeled upon the same main pipe point
  when the DCache/DTag get written directly on D fills), but instead when CP
  confirms that the ITag write is committed enough to let CC restart.
  Test cachennasty5_var_dr_1 accidentally noticed.

```

```

-----
revision 1.85
date: 1995/06/06 02:17:10; author: mws; state: Exp; lines: +9 -4
cc/cc_latedirty.Veqn cc/cc.V cc/cc_control_blob.pim:
  On latedirty cases that CC calls "ahd" (store issues at later time than
  instr causing D miss), the start vldStr were correctly pipelined to R16
  and R18 for cc_latedirty.Veqn to examine but not the match result which
  was staged to R14 only then used in R16 and R18. This caused matches
  from the cyl number 2 higher for the -2 case and 4 higher for the -4 case
  to be used instead of our own cylinder. Test hermnasty_1 accidentally
  noticed. Fix in cc.V 1.83 was probably never right but just perturbed
  cachesynchnasty2_var_a_1 enough to make it pass.
cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.
  Also note that ccrcv.Veqn 51.7 logmsg should have noted that
  it was making the I inprog release 10 ticks later as it already was in
  the D case to prevent CC from absorbing a new D miss too quickly after
  an I miss finished. The new D miss would retrigger the still piping
  later vldFillR21 causing the fillcount to get out of synch with the rest
  of CC, allowing CC to think it was done 1 hexlet early on later fills
  and clobber registers holding the write data for the 4th hexlet fill.
  Test exintbash_var_a_1 accidentally noticed.

```

```

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc_control_blob.pim,v
Working file: verilog/bsrc/cc/cc_control_blob.pim
head: 77.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 2
description:

```

```

-----
revision 77.7
date: 1995/06/07 22:28:58; author: mws; state: Exp; lines: +32 -32
cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active. This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry. Delays in

```

the fill writes navigating through NB+CP allowed the fill adrs to change 1st. So change CC to release inprog(p1) not when it sees the last I fill hexlet get stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart. Test cachennasty5_var_dr_1 accidentally noticed.

revision 77.6

date: 1995/06/06 02:17:13; author: mws; state: Exp; lines: +11 -9

cc/cclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:

On latedirty cases that CC calls "ahd" (store issues at later time than instr causing D miss), the start vldStr were correctly pipelined to R16 and R18 for cclatedirty.Veqn to examine but not the match result which was staged to R14 only then used in R16 and R18. This caused matches from the cyl number 2 higher for the -2 case and 4 higher for the -4 case to be used instead of our own cylinder. Test hermnasty_1 accidentally noticed. Fix in cc.V 1.83 was probably never right but just perturbed cachesynchnasty2_var_a_1 enough to make it pass.

cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.

Also note that ccrcv.Veqn 51.7 logmsg should have noted that it was making the I inprog release 10 ticks later as it already was in the D case to prevent CC from absorbing a new D miss too quickly after an I miss finished. The new D miss would retrigger the still piping later vldFillR21 causing the fillcount to get out of synch with the rest of CC, allowing CC to think it was done 1 hexlet early on later fills and clobber registers holding the write data for the 4th hexlet fill. Test exintbash_var_a_1 accidentally noticed.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cclatedirty.Veqn,v

Working file: verilog/bsrc/cc/cclatedirty.Veqn

head: 40.9

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 9; selected revisions: 1

description:

revision 40.9

date: 1995/06/06 02:17:14; author: mws; state: Exp; lines: +13 -5

cc/cclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:

On latedirty cases that CC calls "ahd" (store issues at later time than instr causing D miss), the start vldStr were correctly pipelined to R16 and R18 for cclatedirty.Veqn to examine but not the match result which was staged to R14 only then used in R16 and R18. This caused matches from the cyl number 2 higher for the -2 case and 4 higher for the -4 case to be used instead of our own cylinder. Test hermnasty_1 accidentally noticed. Fix in cc.V 1.83 was probably never right but just perturbed cachesynchnasty2_var_a_1 enough to make it pass.

cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.

Also note that ccrcv.Veqn 51.7 logmsg should have noted that it was making the I inprog release 10 ticks later as it already was in the D case to prevent CC from absorbing a new D miss too quickly after an I miss finished. The new D miss would retrigger the still piping later vldFillR21 causing the fillcount to get out of synch with the rest of CC, allowing CC to think it was done 1 hexlet early on later fills

and clobber registers holding the write data for the 4th hexlet fill.
Test exintbash_var_a_1 accidentally noticed.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccrcv.Veqn,v

Working file: verilog/bsrc/cc/ccrcv.Veqn

head: 51.10

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 10; selected revisions: 3

description:

revision 51.9

date: 1995/06/07 22:29:00; author: mws; state: Exp; lines: +42 -65

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:

A cylinder doing an I fill interrupted away so that forward progress became active. This allowed another cyl to start a new I miss, which reloaded the saved GVA needed to write the original miss's ITag entry. Delays in the fill writes navigating through NB+CP allowed the fill adrs to change 1st. So change CC to release inprog(p1) not when it sees the last I fill hexlet get stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart.

Test cachennasty5_var_dr_1 accidentally noticed.

revision 51.8

date: 1995/06/06 02:17:16; author: mws; state: Exp; lines: +57 -5

cc/ccclatedirty.Veqn cc/cc.V cc/cc_control_blob.pim:

On latedirty cases that CC calls "ahd" (store issues at later time than instr causing D miss), the start vldStr were correctly pipelined to R16 and R18 for cclatedirty.Veqn to examine but not the match result which was staged to R14 only then used in R16 and R18. This caused matches from the cyl number 2 higher for the -2 case and 4 higher for the -4 case to be used instead of our own cylinder. Test hermnasty_1 accidentally noticed. Fix in cc.V 1.83 was probably never right but just perturbed cachesynchnasty2_var_a_1 enough to make it pass.

cc/ccrcv.Veqn: Add some comments explaining why CC releases when it does.

Also note that ccrcv.Veqn 51.7 logmsg should have noted that

it was making the I inprog release 10 ticks later as it already was in the D case to prevent CC from absorbing a new D miss too quickly after an I miss finished. The new D miss would retrigger the still piping later vldFillR21 causing the fillcount to get out of synch with the rest of CC, allowing CC to think it was done 1 hexlet early on later fills and clobber registers holding the write data for the 4th hexlet fill.

Test exintbash_var_a_1 accidentally noticed.

revision 51.7

date: 1995/06/06 00:19:28; author: billz; state: Exp; lines: +9 -18

I and D states transition from vldFillR21 signal. vldFillR11 is used only in D miss processing to predecode twall (tag write, all bits).

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119; selected revisions: 2
description:
releasebom adding BOM

revision 58.0
date: 1995/06/07 22:31:50; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
 A cylinder doing an I fill interrupted away so that forward progress became
 active. This allowed another cyl to start a new I miss, which reloaded
 the saved GVA needed to write the original miss's ITag entry. Delays in
 the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
 So change CC to release inprog(p1) not when it sees the last I fill hexlet get
 stuffed into NB (which was arbitrarily modeled upon the same main pipe point
 when the DCache/DTag get written directly on D fills), but instead when CP
 confirms that the ITag write is committed enough to let CC restart.
 Test cachena5_var_dr_1 accidentally noticed.

revision 57.1
date: 1995/06/07 22:31:43; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.power.tab.top,v
Working file: verilog/bsrc/cp/cp.power.tab.top
head: 19.12

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:

revision 19.12
date: 1995/06/07 22:28:47; author: mws; state: Exp; lines: +1 -1
cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
 A cylinder doing an I fill interrupted away so that forward progress became
 active. This allowed another cyl to start a new I miss, which reloaded
 the saved GVA needed to write the original miss's ITag entry. Delays in
 the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
 So change CC to release inprog(p1) not when it sees the last I fill hexlet get
 stuffed into NB (which was arbitrarily modeled upon the same main pipe point
 when the DCache/DTag get written directly on D fills), but instead when CP

confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cpl.pim,v

Working file: verilog/bsrc/cp/cpl.pim

head: 41.7

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 7; selected revisions: 1

description:

revision 41.6

date: 1995/06/07 22:28:49; author: mws; state: Exp; lines: +1 -1

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:

A cylinder doing an I fill interrupted away so that forward progress became active. This allowed another cyl to start a new I miss, which reloaded the saved GVA needed to write the original miss's ITag entry. Delays in the fill writes navigating through NB+CP allowed the fill adrs to change 1st. So change CC to release inprog(pl) not when it sees the last I fill hexlet get stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v

Working file: verilog/bsrc/gt/BOM

head: 98.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 194; selected revisions: 2

description:

releasebom adding BOM

revision 96.0

date: 1995/06/03 14:49:03; author: woody; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the gtlb. gt placement updated. The 2 vref generators are placed in the row immed below the gtlb with one on each side of the clockspar in the middle of the gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

revision 95.1

date: 1995/06/03 14:48:56; author: woody; state: Exp; lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/Makefile,v
Working file: verilog/bsrc/gt/Makefile
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29; selected revisions: 1
description:

revision 1.29

date: 1995/06/03 14:45:38; author: woody; state: Exp; lines: +2 -2
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/clean-request,v
Working file: verilog/bsrc/gt/clean-request
head: 41.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8; selected revisions: 1
description:

revision 41.8

date: 1995/06/03 14:45:40; author: woody; state: Exp; lines: +2 -1
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gt.V,v
Working file: verilog/bsrc/gt/gt.V
head: 2.28
branch:
locks: strict
access list:
keyword substitution: kv

```

total revisions: 28;    selected revisions: 1
description:
-----
revision 2.27
date: 1995/06/03 14:45:42;  author: woody;  state: Exp;  lines: +9 -2
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/pimlib.pl,v
Working file: verilog/bsrc/gt/pimlib.pl
head: 26.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
-----
revision 26.23
date: 1995/06/03 14:45:44;  author: woody;  state: Exp;  lines: +13 -1
Changes to euterpe.V and gt.V to accomadate for the 2 added vref signals to the
gtlb. gt placement updated. The 2 vref generators are placed in the row immed
below the gtlb with one on each side of the clockspar in the middle of the
gtlb.

Requires proteus/ged/gt/BOM 10.0 and proteus/verilog/src/gt/BOM 8.0 to run
verilog.

5woody_0 fabbed with both the behavioral model and the real gtlb.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 110.0
date: 1995/06/07 22:34:23;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

```



```
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active. This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry. Delays in
  the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
  So change CC to release inprog(p1) not when it sees the last I fill hexlet get
  stuffed into NB (which was arbitrarily modeled upon the same main pipe point
  when the DCache/DTag get written directly on D fills), but instead when CP
  confirms that the ITag write is committed enough to let CC restart.
  Test cachenas5_var_dr_1 accidentally noticed.
```

```
-----
revision 109.1
date: 1995/06/06 18:01:36; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc
      hc0_control.pim
```

```
Move usnapi2/u0 to avoid a toplevel collision
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0_control.pim,v
Working file: verilog/bsrc/hc/hc0_control.pim
head: 73.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25; selected revisions: 1
description:
-----
```

```
revision 73.17
date: 1995/06/06 18:01:08; author: woody; state: Exp; lines: +3 -1
Move usnapi2/u0 to avoid a toplevel collision
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480; selected revisions: 2
description:
-----
```

```
revision 203.0
date: 1995/06/07 22:38:30; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \
cp/cp.power.tab.top cp/cpl.pim \
euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \
uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:
  A cylinder doing an I fill interrupted away so that forward progress became
  active. This allowed another cyl to start a new I miss, which reloaded
  the saved GVA needed to write the original miss's ITag entry. Delays in
  the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
  So change CC to release inprog(p1) not when it sees the last I fill hexlet get
```

stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

revision 202.1

date: 1995/06/07 22:38:18; author: mws; state: Exp; lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

Working file: verilog/bsrc/uu/uu.V

head: 1.202

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 202; selected revisions: 1

description:

issue unit

revision 1.191

date: 1995/06/07 22:29:35; author: mws; state: Exp; lines: +6 -6

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:

A cylinder doing an I fill interrupted away so that forward progress became active. This allowed another cyl to start a new I miss, which reloaded the saved GVA needed to write the original miss's ITag entry. Delays in the fill writes navigating through NB+CP allowed the fill adrs to change 1st. So change CC to release inprog(p1) not when it sees the last I fill hexlet get stuffed into NB (which was arbitrarily modeled upon the same main pipe point when the DCache/DTag get written directly on D fills), but instead when CP confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.power.tab.top,v

Working file: verilog/bsrc/uu/uu.power.tab.top

head: 119.13

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 13; selected revisions: 1

description:

revision 119.13

date: 1995/06/07 22:29:45; author: mws; state: Exp; lines: +3 -3

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:

A cylinder doing an I fill interrupted away so that forward progress became active. This allowed another cyl to start a new I miss, which reloaded the saved GVA needed to write the original miss's ITag entry. Delays in

the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
So change CC to release inprog(p1) not when it sees the last I fill hexlet get
stuffed into NB (which was arbitrarily modeled upon the same main pipe point
when the DCache/DTag get written directly on D fills), but instead when CP
confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v

Working file: verilog/bsrc/uu/uu_control.pim

head: 68.60

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 60; selected revisions: 1

description:

revision 68.56

date: 1995/06/07 22:30:07; author: mws; state: Exp; lines: +1 -1

cc/ccrcv.Veqn cc/cc.V cc/cc_control_blob.pim \

cp/cp.power.tab.top cp/cpl.pim \

euterpe.V (incl UUvldSN128WrtR10 UUvldSN128WrtDR10 name/function change) \

uu/uu.V uu/uu.power.tab.top uu/uu_control.pim:

A cylinder doing an I fill interrupted away so that forward progress became
active. This allowed another cyl to start a new I miss, which reloaded
the saved GVA needed to write the original miss's ITag entry. Delays in
the fill writes navigating through NB+CP allowed the fill adrs to change 1st.
So change CC to release inprog(p1) not when it sees the last I fill hexlet get
stuffed into NB (which was arbitrarily modeled upon the same main pipe point
when the DCache/DTag get written directly on D fills), but instead when CP
confirms that the ITag write is committed enough to let CC restart.
Test cachena5_var_dr_1 accidentally noticed.

=====